WHAT IS CLAIMED IS:

1. A repeater inserted in a signal transmission line, comprising first and second logic gates cascaded in this order along a direction of a signal transmission in the signal transmission line, each of said first and second logic gate having a logic inverting function, said first logic gate having a current driveability than a current driveability of said second logic gate.

2. The repeater according to claim 1, wherein said repeater is inserted in a clock distribution line as said signal transmission line.

3. A semiconductor device comprising a signal transmission line and a plurality of repeaters inserted in said signal transmission line to divide said signal transmission line into a plurality of divided signal lines, each of said repeaters comprising first and second logic gates cascaded in this order along a direction of a signal transmission in said signal transmission line, each of said first and second logic gates having a logic inverting function, said first logic gate having a current driveability than a current driveability of said second logic gate.

4. The semiconductor device according to claim 3, wherein each of said divided signal lines is longer than an internal signal line connecting together said first and second inverters in each of said repeater.

5. The semiconductor device according to claim 3, further comprising

a branch signal line and another repeater having an input connected to said branch line, said another repeater comprising third and fourth logic gates cascaded in this order and having a logic inverting function, said third logic gate having a current driveability than a current driveability of said fourth logic gate, one of said repeaters having an output connected to an input of another of said repeaters through one of said divided signal lines and said another repeater through said branch signal line.

6. The semiconductor device according to claim 5, wherein said signal transmission line is a clock distribution line.